



- Analysis of Signals on Digital Metallic Line for ISDN-Basic-Access -

Recommendation G.961 from ITU-T (ex-CCITT) defines in Appendix II the core requirements for a Echo Cancellation system using 2B1Q line code.

1. ANALYSIS PRINCIPLE

Clarinet ISDN uses, to analyse and simulate 2B1Q line code, two widely used MOTOROLA MC145572 chips.

The first chip simulates a NT1 (user), and the second chip simulates a LT (network). In Serial Monitoring the two chips are used. In Monitoring or User mode, the first chip synthesizes clocks for Clarinet ISDN.

The indications provided by the chips are the state of the line and the M4 bits of the multiframe:

- ACT: SN3 and SL3 with data transparency
- SYN: SN3 and SL3, but loss of data transparency
- ---: state other than ACT, SYN, IDLE
- IDLE: no signal, SN0 or SL0
- M4 bit from LT to NT1: ACT, DEA, UOA, AIB,
- M4 bit from NT1 to LT: ACT, PS1, PS2, NTM, CSO, SAI.

The line system is fully active when we have the indications:

- ACT on NT and LT sides
- From LT ACT = 1, DEA = 1, UOA = 1
- From NT ACT = 1, SAI = 1

2. USER (NT1) AND NETWORK (LT) MODE

In Network (LT) or User (NT1) mode, after the MONITORING ON indication, the simulation chip leaves the reset state and can only process a COLD Start. If the connected equipment has enabled WARM Start, the first activation could fail, in this case the line system will be activated on the second attempt.

3. SERIAL MONITORING MODE

At the first execution of a MONITORING profile, after the MONITORING ON indication, the NT and LT chips leaves the reset state and can only process a COLD Start. If a connected equipment have enabled WARM Start, its first activation could fail, in this case the line system will be activated on the second attempt.

If the NT side is active before the LT side, the synchronization of CLARINET clock when the LT side becomes active could desynchronize the NT side.

Between two executions of a MONITORING profile, the line monitoring is still active and follows the states of the LT and NT sides, but no events are generated.

4. EXAMPLE OF ACTIVATION IN USER MODE (NT1)

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17:14:19/042.8 1-  NT: ---  »LT: IDL
17:14:19/042.8 1- »NT: IDL   LT: IDL
17:14:19/085.1 1-  NT: IDL  »LT: ---
17:14:21/886.7 1-  NT: IDL  »LT: ACT
17:14:21/886.7 1- »NT: ACT   LT: ACT
17:14:21/886.8 1-  NT »ACT:1  »PS1:1  »PS2:1  »NTM:1  CSO:0  »SAI:1
17:14:21/901.8 1-  LT »ACT:0  »DEA:1  »UOA:1  »AIB:1
17:14:30/565.5 1-  LT »ACT:1  DEA:1   UOA:1   AIB:1

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5. EXAMPLE OF ACTIVATION IN NETWORK MODE (LT)

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18:36:10/045.1 1-  NT: ---  »LT: IDL
18:36:10/045.1 1- »NT: IDL   LT: IDL
18:36:10/094.7 1- »NT: ---   LT: IDL
18:36:17/250.1 1- »NT: ACT   LT: IDL
18:36:17/250.1 1-  NT: ACT  »LT: ACT
18:36:17/250.1 1-  LT »ACT:0  »DEA:1  »UOA:1  »AIB:1
18:36:17/262.1 1- »NT: SYN   LT: ACT
18:36:17/262.1 1-  NT: SYN  »LT: SYN
18:36:23/505.4 1- »NT: ACT   LT: SYN
18:36:23/505.4 1-  NT: ACT  »LT: ACT
18:36:23/505.4 1-  NT »ACT:0  »PS1:1  »PS2:1  »NTM:1  CSO:0  »SAI:0
18:36:35/905.4 1-  NT »ACT:1  PS1:1   PS2:1   NTM:1  CSO:0  »SAI:1
18:36:35/905.5 1-  LT »ACT:1  DEA:1   UOA:1   AIB:1

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6. EXAMPLE OF ACTIVATION IN SERIAL MONITORING

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17:50:12/587.1 1- »NT: IDL   LT: IDL
17:50:12/587.8 1-  NT: IDL  »LT: ---
17:50:15/329.7 1-  NT: IDL  »LT: ACT
17:50:15/335.5 1- »NT: ---   LT: ACT
17:50:15/344.6 1-  LT »ACT:0  »DEA:1  »UOA:1  »AIB:1
17:50:15/452.4 1- »NT: ACT   LT: ACT
17:50:15/476.3 1-  NT »ACT:1  »PS1:1  »PS2:0  »NTM:1  »CSO:0  »SAI:1
17:50:15/486.8 1- »NT: SYN   LT: ACT
17:50:15/518.4 1- »NT: ---   LT: ACT
17:50:15/998.4 1- »NT: IDL   LT: ACT
17:50:16/045.8 1- »NT: ---   LT: ACT
17:50:24/075.7 1- »NT: ACT   LT: ACT
17:50:24/089.7 1-  NT »ACT:1  »PS1:1  »PS2:0  »NTM:1  »CSO:0  »SAI:1
17:50:24/140.5 1-  LT »ACT:1  DEA:1   UOA:1   AIB:1

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7. CONCLUSION

Clarinet ISDN being dependant on the MC145572 chip cannot be a true layer 1 analyser on Digital Metallic Line for Basic-Rate Access, but indications provided concerning layer 1 are generally sufficient for upper layer interpretation.